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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,621	06/09/2000	Vidyabhusan Gupta	99-LJ-186	3053

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,621	GUPTA, VIDYABHUSAN	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicant's Amendment and Response ("Amendment") to Office Action dated May 20, 2004, faxed October 18, 2005.

1-1. Claims 1-29 are pending.

1-2. Claims 1-29 have been examined and rejected.

Drawings

2. The objection to the drawings has been withdrawn.

Specification

3. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

3-1. It appears that "processing system 10", as described in line 19 of page 20, should be "processing system 100".

Recommendations

4. Claim 8 recites "A method of designing an embedded processing system" in the preamble. For clarification purposes, the Examiner suggests that "A method of designing an embedded processing system" be replaced with "A method of designing a memory configuration for use in an embedded processing system".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Giorgi et al., "An Educational Environment for Program Behavior Analysis and Cache Memory Design", 1997 Frontiers in Education Conference, Proceedings of Teaching and Learning in an Era of Change, 1997, Volume 3, pages 1243-1248.

6-1. Regarding claim 1, Giorgi et al. disclose an apparatus for designing a memory for use in an embedded processing system comprising:

a simulation controller capable of simulating execution of a test program to be executed by said embedded processing system (Applications can be executed and debugged on a dedicated ARM instruction set simulator, page 1244, left column, paragraph 3; cjpeg program, page 1246, right column, paragraph 2);

a memory access monitor capable of monitoring memory accesses to a simulated memory space during said simulated execution of said test program, wherein said memory access monitor is capable of generating memory usage statistical data associated with said monitored memory accesses, and wherein said memory accesses comprise read operations and write operations (Program Behavior Analysis, page 1244, left column, paragraph 5; traces the execution of the cjpeg program, page 1246, right column, paragraph 2); and

a memory optimization controller capable of comparing said memory usage statistical data and one or more design criteria associated with said embedded processing system (for example, the image compression be completed in less than 1s, page 1246, right column, paragraph 2) and, in response to said comparison, determining at least one memory configuration capable of satisfying said one or more design criteria (select a configuration that best meets cost-effectiveness and performance requirements, page 1247, left column, paragraph 4, through page 1247, right column, paragraph 2).

6-2. Regarding claim 2, Giorgi et al. further disclose said at least one memory configuration is determined from a set of memory types, said ' set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM) (for example, a 1-Mbyte memory DRAM bank, a 128-Kbyte memory PROM bank, page 1246, right column, paragraph 3).

6-3. Regarding claim 3, Giorgi et al. further disclose said at least one memory configuration comprises a first memory type and a first memory size associated with said first memory type (For each module, the configuration parameters include the module type, the starting address and the size, page 1246, right column, paragraph 7).

6-4. Regarding claim 4, Giorgi et al. further disclose said at least one memory configuration further comprises a second memory type and a second memory size associated with said second memory type (For each module, the configuration parameters include the module type, the starting address and the size, page 1246, right column, paragraph 7).

6-5. Regarding claim 5, Giorgi et al. further disclose said simulation controller simulates execution of said program N times and wherein said memory access monitor monitors said memory accesses during said N simulated executions of said program and generates said memory usage statistical data based on said N simulated executions of said program (trace analysis, page 1244, left column, paragraph 5; allows the cache to exit its cold state and to reach a steady condition, page 1244, right column, paragraph 2).

6-6. Regarding claim 6, Giorgi et al. further disclose said memory optimization controller is further capable of determining at least one figure of merit associated with said at least one memory configuration, wherein said at least one figure of merit indicates a degree to which said at least one memory configuration satisfies said one or more design criteria (for example, max delay as shown in Table 1 at page 1248 can be used as figure of merit to select a configuration for rawcaudio program).

6-7. Regarding claim 7, Giorgi et al. further disclose comprising a code optimization controller capable of modifying said program in response to said comparison of said memory usage statistical data and said one or more design criteria to thereby enable said embedded processing system to execute said test program according to said one or more design criteria (cache scheme defined by, for example, the mapping policy, the replacement algorithm, page 1245, right column, paragraph 2).

6-8. Regarding claims 8-14, these method claims include equivalent apparatus limitations as in claims 1-7 and are anticipated using the same analysis of claims 1-7.

6-9. Regarding claims 15-21, these system claims include equivalent apparatus limitations as in claims 1-7 and are anticipated using the same analysis of claims 1-7.

6-10. Regarding claims 22-28, these medium claims include equivalent apparatus limitations as in claims 1-7 and are anticipated using the same analysis of claims 1-7.

6-11. Regarding claim 29, Giorgi et al. further disclose the memory usage statistical data comprises at least one of:

one or more first histograms based on variable names contained in the program to be executed by the embedded processing system; and

one or more second histograms based on memory locations accessed by the program to be executed by the embedded processing system (page 1245, Figure 2).

Applicant's Arguments

7. Applicant argues the following:

7-1. Rejections Under 35 U.S.C. §112

(1) "The question is whether the concepts and structures expressed by these words appear in the specification. The Applicant respectfully submits that they do" (page 15, paragraph 1, Amendment).

7-2. Rejections Under 35 U.S.C. §103

(2) The Gupta reference does not disclose all the recited limitations and the supposed motivation to combine references is legally insufficient (pages 18-26, Amendment).

Response to Arguments

8. Applicant's arguments have been fully considered.

8-1. Applicant's argument (1) is persuasive. The rejections of claims 1-29 under 35 U.S.C. 112, first paragraph, in Office Action dated May 20, 2004, have been withdrawn.

8-2. Applicant's argument (2) is moot in view of the new ground(s) of rejection. The rejections of claims 1-29 under 35 U.S.C. 103(a) in Office Action dated May 20, 2004, have been withdrawn.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Coumeri et al., "Memory Modeling for System Synthesis", Proceedings of 1998 International Symposium on Low Power Electronics and Design, August 1998, pages 179-184, is cited as disclosing methodology for developing memory models of on-chip SRAM memory organizations using weighted stepwise linear regression.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
January 9, 2006

Thai Phan
Patent Examiner
Au: 2128